

# NTJD4158C, NVJD4158C

## Small Signal MOSFET

30 V/–20 V, +0.25/–0.88 A,  
Complementary, SC–88

### Features

- Leading 20 V Trench for Low  $R_{DS(on)}$  Performance
- ESD Protected Gate
- SC–88 Package for Small Footprint (2 x 2 mm)
- NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- DC–DC Conversion
- Load/Power Management
- Load Switch
- Cell Phones, MP3s, Digital Cameras, PDAs

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain–to–Source Voltage	N–Ch	$V_{DSS}$	30	V	
	P–Ch		–20		
Gate–to–Source Voltage	N–Ch	$V_{GS}$	$\pm 20$	V	
	P–Ch		$\pm 12$		
N–Channel Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	0.25	A
				$T_A = 85^\circ\text{C}$	
P–Channel Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	–0.88	A
				$T_A = 85^\circ\text{C}$	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	0.27	W
Pulsed Drain Cur- rent	N–Ch	$t_p = 10 \mu\text{s}$	$I_{DM}$	0.5	A
	P–Ch			–3.0	
Operating Junction and Storage Temperature			$T_J, T_{stg}$	–55 to 150	$^\circ\text{C}$
Source Current (Body Diode)	N–Ch	$I_S$	0.25	A	
	P–Ch		–0.48		
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			$T_L$	260	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction–to–Ambient – Steady State (Note 1)	$R_{\theta JA}$	460	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

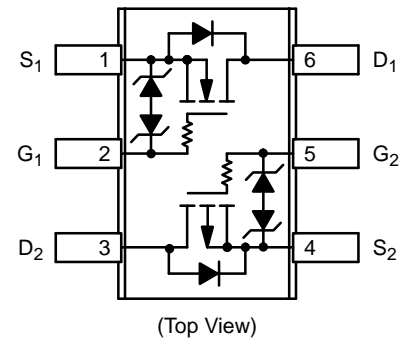


ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	$I_D$ Max
N–Ch 30 V	1.0 $\Omega$ @ 4.5 V	0.25 A
	1.5 $\Omega$ @ 2.5 V	
P–Ch –20 V	215 m $\Omega$ @ –4.5 V	–0.88 A
	345 m $\Omega$ @ –2.5 V	

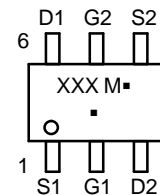
SC–88 (SOT–363)  
(6–Leads)



### MARKING DIAGRAM & PIN ASSIGNMENT



SC–88 (SOT–363)  
CASE 419B  
STYLE 26



XXX = Specific Device Code  
M = Date Code  
▪ = Pb–Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# NTJD4158C, NVJD4158C

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS (Note 3)</b>							
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	N	V <sub>GS</sub> = 0 V	I <sub>D</sub> = 250 μA	30		V
		P		I <sub>D</sub> = -250 μA	-20		
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	N			33		mV/°C
		P			-9.0		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	N	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 30 V	T <sub>J</sub> = 25°C		1.0	μA
		P	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -16 V			1.0	
		N	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 30 V	T <sub>J</sub> = 125°C		0.5	
		P	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -16 V			0.5	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	N	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 10 V			1.0	μA
		P	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = -4.5 V			1.0	

## ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	N	V <sub>GS</sub> = V <sub>DS</sub>	I <sub>D</sub> = 100 μA	0.8	1.2	1.5	V
		P		I <sub>D</sub> = -250 μA	-0.45			
Negative Gate Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>	N				3.2		mV/°C
		P				-2.7		
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	N	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 mA			1.0	1.5	Ω
		P	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -0.88 A			0.215	0.260	
		N	V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 10 mA			1.5	2.5	
		P	V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -0.71 A			0.345	0.500	
Forward Transconductance	g <sub>FS</sub>	N	V <sub>DS</sub> = 3.0 V, I <sub>D</sub> = 10 mA			0.08		S
		P	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -0.88 A			3.0		

## CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	N	f = 1 MHz, V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 5.0 V		20	33	pF	
		P		V <sub>DS</sub> = -20 V		155	225		
Output Capacitance	C <sub>OSS</sub>	N		V <sub>DS</sub> = 5.0 V		19	32		
		P		V <sub>DS</sub> = -20 V		25	40		
Reverse Transfer Capacitance	C <sub>RSS</sub>	N		V <sub>DS</sub> = 5.0 V		7.25	12		
		P		V <sub>DS</sub> = -20 V		18	30		
Total Gate Charge	Q <sub>G(TOT)</sub>	N		V <sub>GS</sub> = 5.0 V, V <sub>DS</sub> = 24 V, I <sub>D</sub> = 0.1 A		0.9	1.5		nC
		P		V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -10 V, I <sub>D</sub> = -0.88 A		2.2	3.5		
Threshold Gate Charge	Q <sub>G(TH)</sub>	N		V <sub>GS</sub> = 5.0 V, V <sub>DS</sub> = 24 V, I <sub>D</sub> = 0.1 A		0.2			
		P		V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -10 V, I <sub>D</sub> = -0.88 A		0.2			
Gate-to-Source Charge	Q <sub>GS</sub>	N	V <sub>GS</sub> = 5.0 V, V <sub>DS</sub> = 24 V, I <sub>D</sub> = 0.1 A		0.3				
		P	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -10 V, I <sub>D</sub> = -0.88 A		0.5				
Gate-to-Drain Charge	Q <sub>GD</sub>	N	V <sub>GS</sub> = 5.0 V, V <sub>DS</sub> = 24 V, I <sub>D</sub> = 0.1 A		0.2				
		P	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -10 V, I <sub>D</sub> = -0.88 A		0.65				

## SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t <sub>d(ON)</sub>	N	V <sub>GS</sub> = 4.5 V, V <sub>DD</sub> = 5.0 V, I <sub>D</sub> = 250 mA, R <sub>G</sub> = 50 Ω		15		ns	
Rise Time	t <sub>r</sub>				66			
Turn-Off Delay Time	t <sub>d(OFF)</sub>				56			
Fall Time	t <sub>f</sub>				78			
Turn-On Delay Time	t <sub>d(ON)</sub>	P		V <sub>GS</sub> = -4.5 V, V <sub>DD</sub> = -10 V, I <sub>D</sub> = -0.5 A, R <sub>G</sub> = 20 Ω		5.8		
Rise Time	t <sub>r</sub>					6.5		
Turn-Off Delay Time	t <sub>d(OFF)</sub>					13.5		
Fall Time	t <sub>f</sub>					3.5		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	N	V <sub>GS</sub> = 0 V, T <sub>J</sub> = 25°C	I <sub>S</sub> = 10 mA	0.65	0.7	V
		P		I <sub>S</sub> = -0.48 A	-0.8	-1.2	
		N	V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C	I <sub>S</sub> = 10 mA	0.45		
		P		I <sub>S</sub> = -0.48 A	-0.66		
Reverse Recovery Time	t <sub>RR</sub>	N	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 8.0 A/μs	I <sub>S</sub> = 10 mA	12.4		ns
		P	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs	I <sub>S</sub> = -0.48 mA	10.6		

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

3. Switching characteristics are independent of operating junction temperatures.

# NTJD4158C, NVJD4158C

## TYPICAL N-CHANNEL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

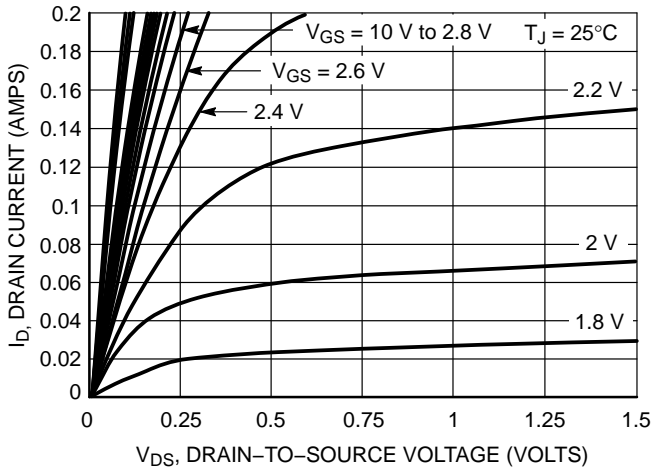


Figure 1. On-Region Characteristics

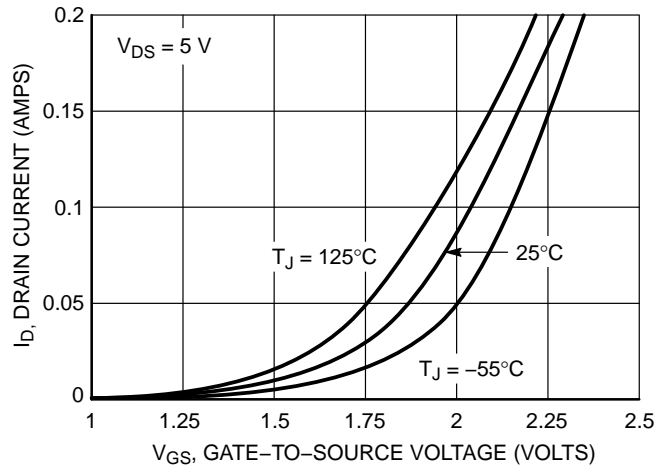


Figure 2. Transfer Characteristics

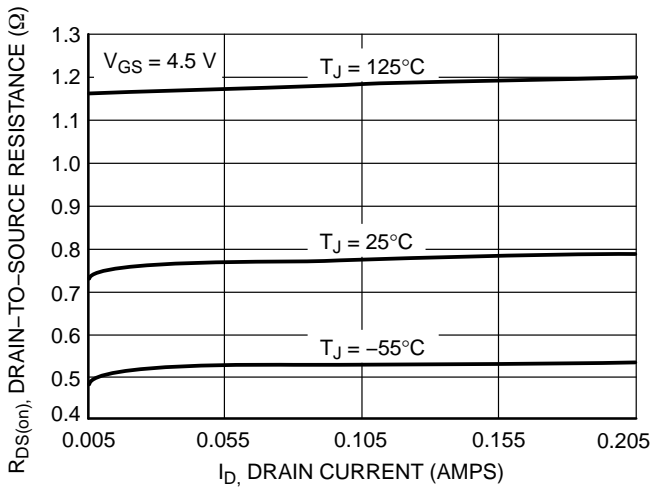


Figure 3. On-Resistance vs. Drain Current and Temperature

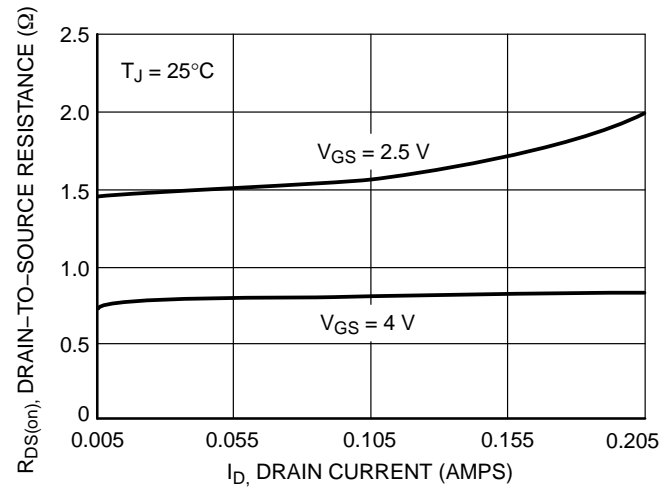


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

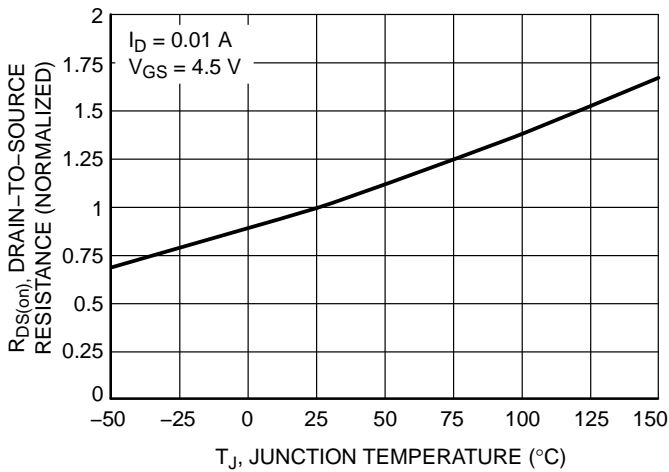


Figure 5. On-Resistance Variation with Temperature

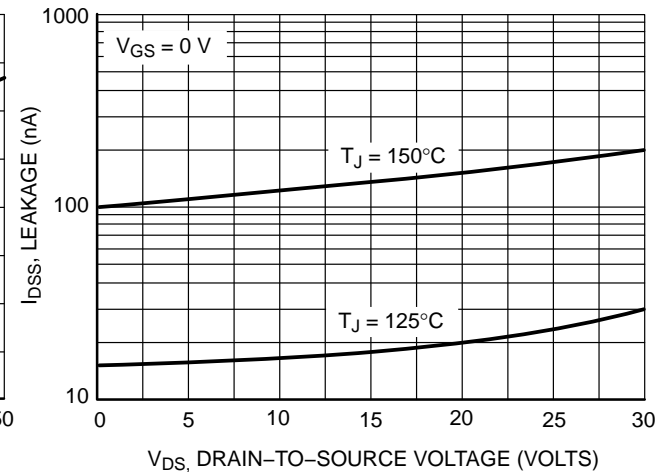
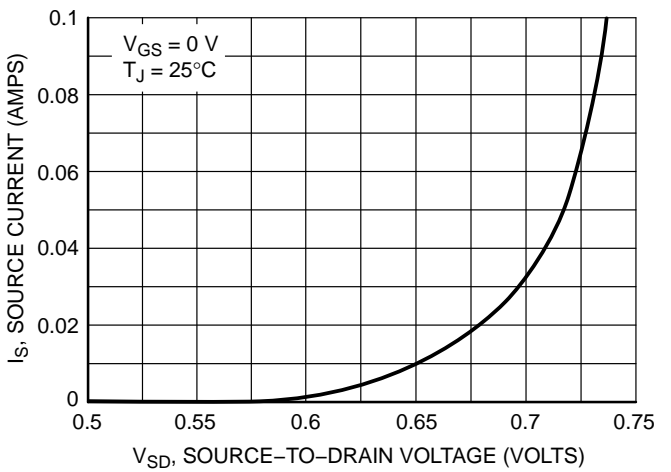
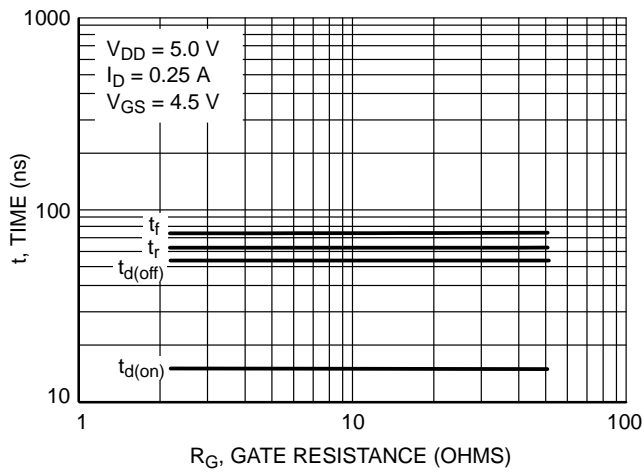
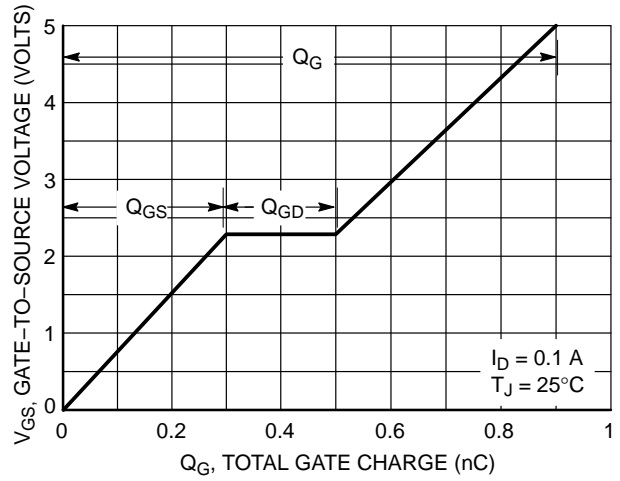
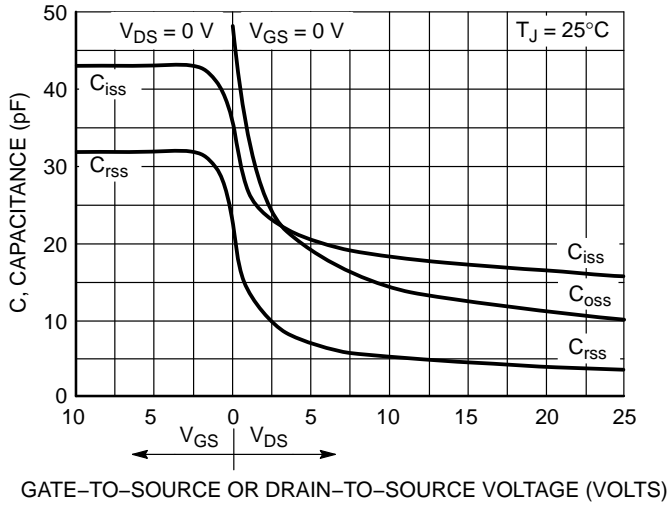


Figure 6. Drain-to-Source Leakage Current vs. Voltage

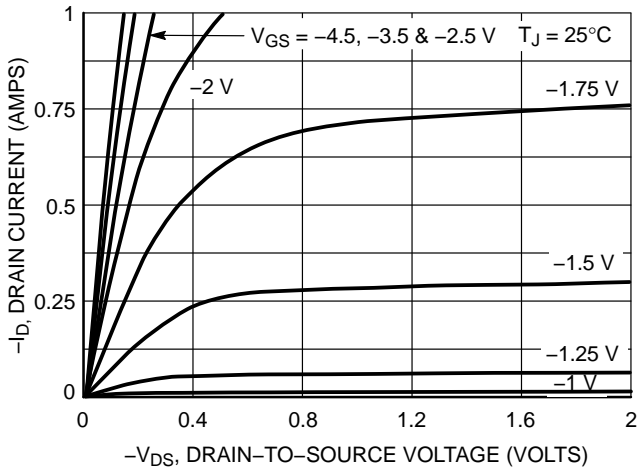
# NTJD4158C, NVJD4158C

## TYPICAL N-CHANNEL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

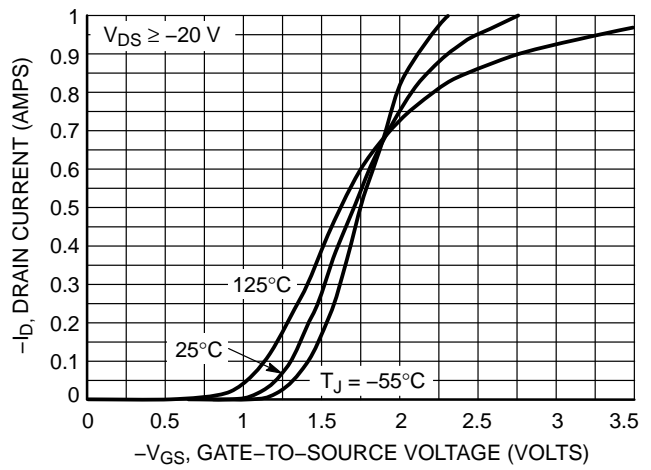


# NTJD4158C, NVJD4158C

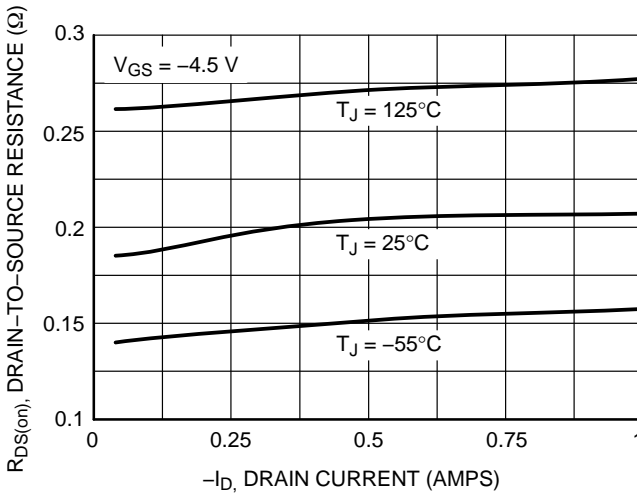
## TYPICAL P-CHANNEL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)



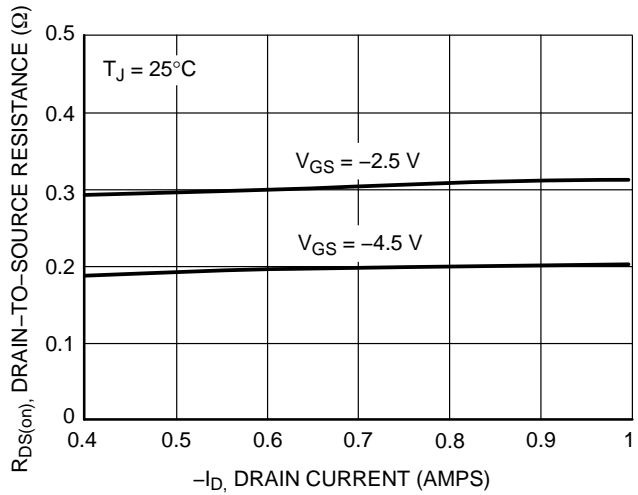
**Figure 1. On-Region Characteristics**



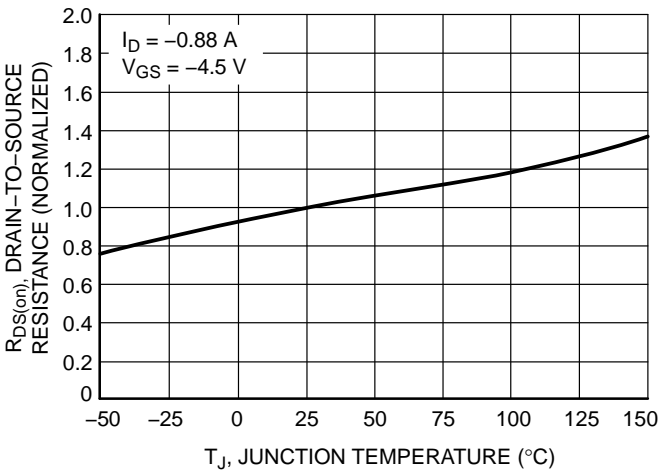
**Figure 2. Transfer Characteristics**



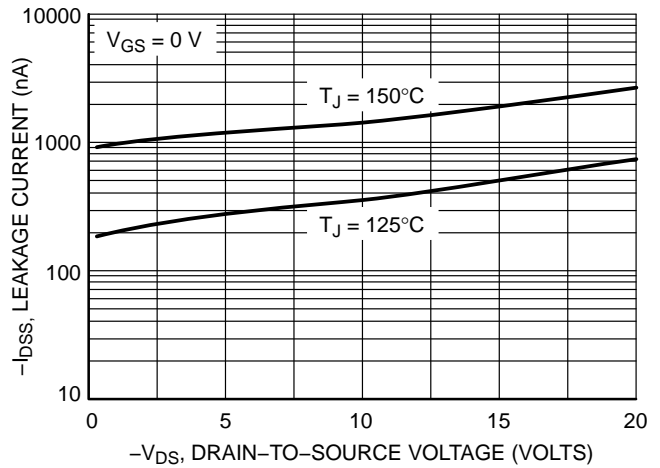
**Figure 3. On-Resistance vs. Drain Current and Temperature**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**



**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current vs. Voltage**

# NTJD4158C, NVJD4158C

## TYPICAL P-CHANNEL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

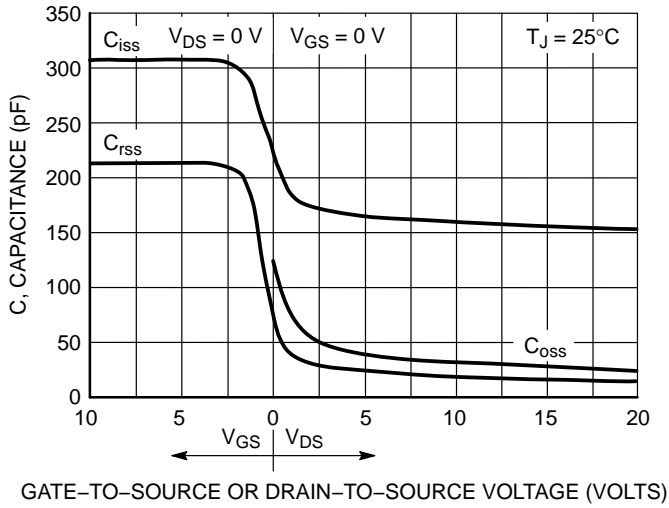


Figure 7. Capacitance Variation

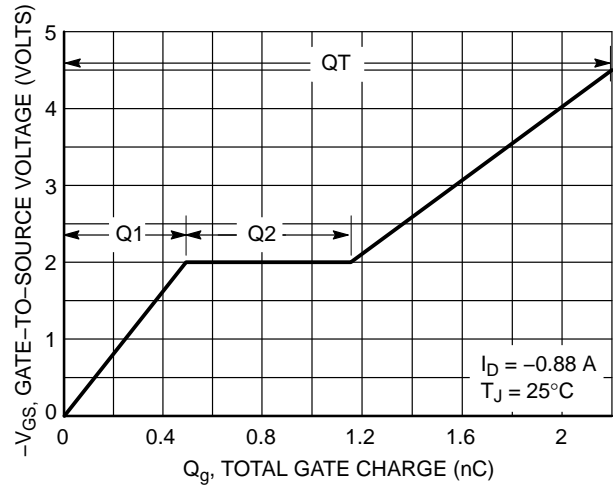


Figure 8. Gate-to-Source Voltage vs. Total Gate Charge

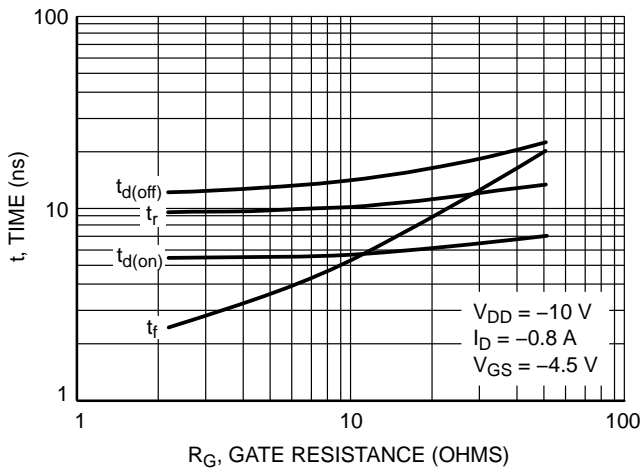


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

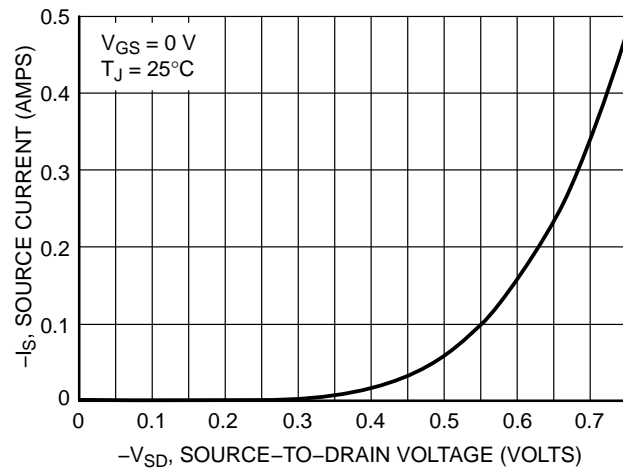


Figure 10. Diode Forward Voltage vs. Current

### ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTJD4158CT1G	TCD	SC-88 (Pb-Free)	3000 / Tape & Reel
NTJD4158CT2G	TCD		
NVJD4158CT1G*	VCD		

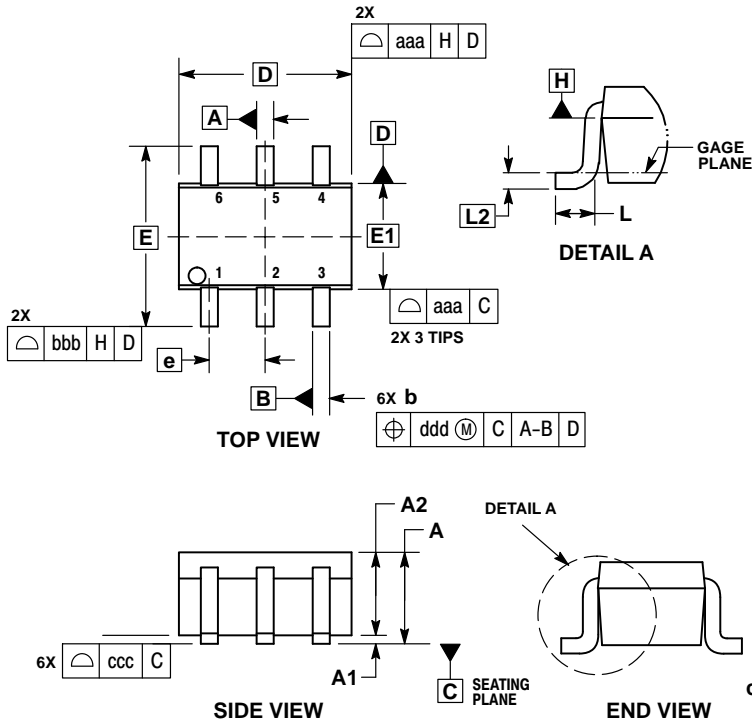
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

# NTJD4158C, NVJD4158C

## PACKAGE DIMENSIONS

SC-88/SC70-6/SOT-363  
CASE 419B-02  
ISSUE Y

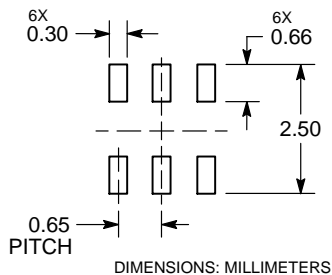


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
  4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
  5. DATUMS A AND B ARE DETERMINED AT DATUM H.
  6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
  7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

STYLE 26:  
PIN 1. SOURCE 1  
2. GATE 1  
3. DRAIN 2  
4. SOURCE 2  
5. GATE 2  
6. DRAIN 1

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative